REMARKS

This is in response to the Office Action of 24 July 2003. Claims 17-28 are pending in the application, and Claims 17-28 have been rejected.

No new matter has been added.

In view of the remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to the integration of at least two processors onto a single integrated circuit, or chip, and providing a shared memory arrangement by which each of the at least two integrated processors are able to access various memories. More particularly, the present invention relates to integrating a first and a second processor on an integrated circuit wherein the first processor accesses a first memory through at least one cache memory disposed intermediate the first memory and the first processor, and the at least one cache memory is coupled to the first memory via a first bus, and wherein the second processor is coupled to a second bus and accesses the first memory through a bridge that provides an appropriate interface between the first bus and the second bus, the busses being dissimilar. In various further aspects of the present invention, the first and second processors may operate at different clock frequencies; there may be a direct communication path between the first processor and the second processor; and there may be an additional cache memory disposed between the second processor and the second bus.

Title

Applicants thank the Examiner for accepting and entering the new title for this application (i.e., Memory Sharing Arrangement For An Integrated Multiprocessor System) which was submitted in the previous response.

Rejections under 35 USC 102(e)

Claims 17-28 have been rejected under 35 USC 102(e), as being anticipated by Nakagawa, et al., (US Patent 6,353,863). The Examiner states that all the limitations of all the pending claims are disclosed by Nakagawa, et al.

For at least the reasons set forth below, Applicants respectfully traverse the rejections of Claims 17-28 under 35 USC 102(e), and requests that these rejections be withdrawn.

With respect to independent Claims 17 and 25, the Examiner states that Nakagawa, et al., at Fig. 4; and at col. 8 line 32 through col. 9 line 14, disclose a first processor coupled to an instruction cache and to a data cache. Applicants respectfully assert that Nakagawa, et al., do not provide such a disclosure. In fact, Nakagawa, et al., show a CPU core 414 coupled to an internal memory 418 for the purpose of receiving instructions; and further show a DSP core 403 coupled to an internal memory X 404 for the purpose of receiving instructions (col. 8, line 67 through col. 9, line 3) and to an Internal memory Y 405 (col. 8, line 67 through col. 9, line 3) for the purpose of receiving instructions. There is no showing of CPU core 414 being coupled to a data cache. Similarly, there is no showing of DSP core 403 being coupled to a data cache. All of the pending independent Claims require a first processor coupled to both an instruction cache and to a data cache. Since this limitation is not shown by Nakagawa, et al., Applicants' Claims can not be anticipated by Nakagawa, et al.

Applicants' Claims also recite the limitation of "a first bus coupled to the instruction cache and to the data cache", and further recite limitation of "a first memory coupled to the first bus". There does not appear to be any structure shown or described in Nakagawa, et al., that matches the claimed first bus that is coupled to both the instruction cache, the data cache, and the first memory. Only CPU External RAM 430, and CPU External ROM 431 appear to be suitably characterizable as a "first memory", however, neither of these is coupled as set forth in the Claims. Since this claimed structure is not shown by Nakagawa, et

al., Applicants' Claims can not be anticipated by Nakagawa, et al.

Applicants' Claims also recite the limitation of "a first bus bridge coupled to the first bus and to the second bus, the first bus bridge providing a path for transferring data between the first memory and the second processor". There does not appear to be any structure shown or described in Nakagawa, et al., that matches the recited limitation. Nakagawa, et al., show a CPU/DSP Interface 410, but this does not provide the pathway between the second processor and the first memory as recited in Applicants' Claims. Since this claimed structure is not shown by Nakagawa, et al., Applicants' Claims can not be anticipated by Nakagawa, et al.

Further Applicants' Claims recite the limitation of "a second bus bridge coupled to the second bus and a third bus, the third bus providing a data pathway within the first processor, the second bus bridge providing a path for transferring data between the second memory and the third bus of the first processor". There is no showing in Nakagawa, et al., of any such structural limitation. Applicant's Claims require that the third bus provide a data pathway within the first processor. There is not such structure, or structural equivalent shown by Nakagawa, et al. Since this claimed structure is not shown by Nakagawa, et al., Applicants' Claims can not be anticipated by Nakagawa, et al.

For at least the reasons set forth above, Applicants respectfully assert that the rejections of Claims 17-28 under 35 USC 102(e) are improper and should be withdrawn.

Applicants further submit, that Nakagawa, et al., do not provide any suggestion or motivation for the structure set forth in Applicants' Claims and therefore Applicants' Claims cannot be considered obvious in view thereof.

Conclusion

All of the rejections in the outstanding Office Action of 18 March 2003 have been responded to, and Applicants respectfully submit that the pending Claims 17-28 are now in condition for allowance.

Appl. No. 09/640,729

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Portland, Oregon